Amendments to the Specification:

Please amend the paragraph beginning at page 13, line 9, of the specification as follows:

According to a sixth embodiment of the present invention, an exemplary method of manufacturing the integrated semiconductor device (Fig. 5) illustrated in connection with the fourth embodiment is described. According to this embodiment, implantation is done for n type drain drift layers 10a, 10b and 10c in the same implantation step. Different concentrations for respective n type diffusion layers are achieved by adjustment of the opening area or opening ratio. Specifically, a stripe or mesh resist mask 21 is used as shown in Fig. 6 to implant impurities. The impurity concentration is low in a semiconductor surface layer 13 corresponding to mask portion 21b while the impurity concentration is high in a semiconductor surface layer 11 corresponding to opening 21a. In Fig. 6, the average impurity concentration of semiconductor surface layers respectively of transistors 50a, 50b and 50c has a relation: 50a < 50b < 50c, which means the average impurity concentration of transistor 50c is the highest. Then, as shown in Fig. 7, annealing is done to make the concentration of the implanted part and non-implanted part uniform.